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A Generalized Carrier-Overlapped PWM Method for Neutral-Point Clamped Multilevel Converters

Kui Wang, *Senior Member, IEEE*, Zedong Zheng, *Senior Member, IEEE*, Lie Xu, *Member, IEEE* and Yongdong Li, *Senior Member, IEEE*

***Abstract*—The neutral-point voltage unbalance problem holds back the extensive application of neutral-point clamped (NPC) multilevel converters with more than three voltage levels in industry. Traditional phase-disposition PWM (PDPWM) or nearest-three-vectors (NTV) modulation cannot achieve the voltage balance over the full modulation indexes and load power factors when the voltage level is higher than three. To solve this problem, a novel generalized carrier-based PWM method named carrier-overlapped PWM (COPWM) for NPC multilevel converters is proposed in this paper, which is proven to satisfy the volt-second balance principle. With this modulation method, the average values of all the neutral-point currents are equal to zero in a fundamental period, and so all the dc-link capacitor voltages can be naturally balanced in the ideal and steady-state conditions. In order to simplify its implementation, an equivalent multi-reference modulation method with only one triangular carrier is also derived. Simulation and experimental results on a five-level diode-clamped inverter are presented to verify the proposed modulation method.**

***Index Terms*— Neutral-point clamped multilevel converter; capacitor voltage balance; multi-reference modulation; pulse width modulation (PWM).**

I. INTRODUCTION

Neutral-point clamped (NPC) multilevel converter is a representative topology that has been widely used in industry in the past decades [1] – [5]. With the increased power and voltage demand for motors and inverters year by year, the multilevel topologies with more than three voltage levels have attracted ever increasing attentions, such as five-level active NPC converter [6], stacked multi-cell converter [7], nested NPC converter [8], five-level hybrid-clamped converter [9], symmetric hybrid multilevel converter [10], etc. Compared with NPC multilevel converters, all these topologies need flying capacitors to generate more switching states and voltage levels, which decreases the power density and increase the costs. However, the NPC multilevel converter suffers from the severe dc-link voltage unbalance problem when the voltage level increases to four or more, which hinders it from extensive adoptions in higher voltage applications.

It has been proven that, the four- and five-level NPC converters can only achieve voltage balance within limited power factors and modulation indexes when using the classic phase-disposition PWM (PDPWM) or nearest-three-vectors (NTV) modulation [13] – [15]. Specially, if the inverter operates with unity power factor, the modulation index will be limited within 0.55 [14]. However, for reactive power applications such as STATCOM, the dc-link capacitor voltages can be balanced under both low and high modulation indexes by injecting proper zero-sequence voltage or space vector modulation [16] – [18]. Nevertheless, for active power applications, these methods can only maintain the neutral point (NP) voltages stable under low modulation indexes.

Several approaches have been suggested to solve this problem. For example, two five-level NPC converters are connected back-to-back in [19], [20], while extra hardware balancing circuits are employed in [21], [22]. Nonetheless, these solutions not only make the system more complex, but also increase the cost. Virtual-space-vector (VV) based PWM is a good solution to achieve the NP voltage balance over all the modulation indexes and load power factors [23], [24]. A generalized VV PWM for three-phase *n*-level NPC converters is proposed in [24]. Each virtual vector is generated by more than one switching state to guarantee that the average value of each NP current equals zero in a control period. However, the VV PWM suffers from high number of switching transitions and complex implementation.

In order to simplify the implementation, an equivalent carrier-based PWM method for VV PWM is also proposed in [24] – [26]. Multiple references are compared to a common carrier and the same control signals with VV PWM can be generated [24]. The greatest advantage of this method is that the dc-link capacitor voltage balancing can be achieved in a carrier period for all the modulation indexes and load power factors, and so the dc-link capacitance value can be largely reduced [25].

A capacitor voltage balancing method using redundant states of space vector modulation for five-level diode clamped inverters is proposed in [27], which can balance the four dc-link capacitor voltages at high modulation index and high power factor. Based on this method, an improved capacitor voltage-balancing method is proposed in [28], which can reduce the ripple voltages of the dc-link capacitors and lower the current THD. Both the two methods are based on space vectors and very complex to implement.

Model-predictive control (MPC) is another popular method to balance the capacitor voltages of various multilevel converters by optimizing a cost function [29]−[31]. However, MPC also suffers from many problems, such as large computation burden, uncertain weighting coefficient and inconstant switching frequency.

In fact, the deviation of the average NP currents from zero is the major reason for the NP voltage unbalance. If the average values of each NP current can be controlled zero in a certain period, then all the NP voltages can be balanced [25]. Based on this idea, a new carrier-based PWM method, named carrier-

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Kui Wang, Zedong Zheng, Lie Xu and Yongdong Li are with the State Key Laboratory of Power System, Department of Electrical Engineering, Tsinghua University, Beijing 100084, China. (e-mail: wangkui@tsinghua.edu.cn; zzd@tsinghua.edu.cn; xulie@tsinghua.edu.cn; liyd@tsinghua.edu.cn)

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overlapped PWM (COPWM), is proposed for four-level NPC converters firstly in [32]. The three triangular carriers are not evenly distributed but overlapped with each other, and the amplitudes are also not identical. In doing so, the average values of the two NP currents are proven to be the same in a carrier period and equal zero in a fundamental period, which means the COPWM has the natural voltage balance ability for four-level NPC converters. The success of COPWM in four-level NPC converters encourages the exploring whether it can be extended to NPC converters with more voltage levels.

This paper proposed a geometrical extension method of the four-level COPWM. Started with the two-level modulation method, a set of bended carriers are deduced geometrically to acquire the same time duration for different voltage levels, which ensures the same NP currents under the COPWM method. By further analyzing the average value of the output voltage in a carrier period, the proposed generalized COPWM is proven to satisfy the volt-second balance principle. Moreover, by calculating the average value of each NP current, the COPWM is demonstrated to make the dc-link capacitor voltages become naturally balanced with the fact that the average values of each NP current equal zero in every fundamental period.

The rest of this paper is organized as follows. Section II introduces the geometric construction and theoretical derivation of the generalized COPWM method. The mathematical proof of the natural voltage balance ability is also presented in this section. Section III deduces the equivalent multi-reference modulation method of the COPWM method geometrically to simplify the implementation. Simulation and experimental results on a five-level diode-clamped inverter are presented in Section IV and V. Finally, Section VI outlines the conclusions.

II. The Generalized COPWM for NPC Multilevel Converters

(a) The geometric construction and theoretical derivation of the generalized COPWM method

NPC multilevel converters include many different types of topologies, such as diode-clamped [10], active NPC [11], T-type NPC [12], etc. All of them can be equivalent to a single-pole multi-throw switch. Fig. 1 shows a phase-leg of the diode-clamped multilevel converter and its equivalent circuit. n+1 voltage levels can be acquired by split the dc-link by n identical capacitors. The nominal voltage of each capacitor is assumed E. i_{N1x} to $i_{N(n-1)x}$ are respectively the currents flowing out of n-1 neutral points N_1 to N_{n-1}, i_{ox} is the phase current, and the subscript symbol x denotes phase ***a***, ***b*** or ***c***.

If E is selected as the base voltage value and the negative pole of the dc-link is referred as the zero potential, then the phase voltage reference u_{refx} will range from 0 to n. The time duration of each voltage level in a carrier period is defined as t_{xj} (j = 0, 1, 2, …n).

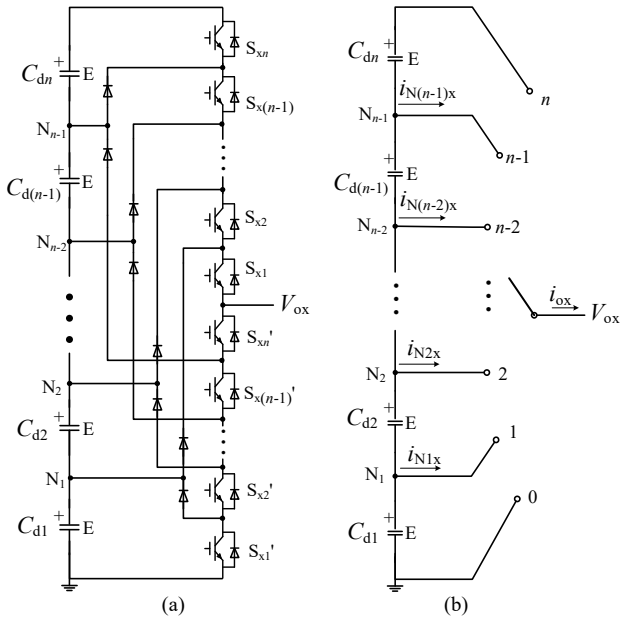

Fig. 1. (a) A phase-leg of the diode-clamped multilevel converter and (b) the equivalent single-pole multi-throw switch circuit.

The phase current flows out of neutral point N_j (j = 1, 2, …, n-1) when the output voltage level is j, so the average NP current in a carrier period can be written as:

$$i_{Njx} = \frac{t_{xj}}{T_s} i_{ox}, j = 1,2,...,n-1 \tag{1}$$

If all the average NP currents equal to zero in a certain period, then the capacitor voltages will remain balanced at the beginning and end of this period. A particular solution is to employ n identical triangular carries (denoted as C_{r0}) with the same amplitude of n, as shown in Fig. 2(a). In doing so, the (n+1)-level NPC converter degenerates into a two-level converter and all the NP currents are equal to zero.

In order to preserve the characteristic of equal NP currents and avoid switching synchronously, the n identical carrier waves should be shifted or varied. A new carrier can be obtained by dragging the two point of the original triangular carrier C_{r0} whose coordinates are (T_s/4, n/2) and (3T_s/4, n/2) (the intersection points of C_{r0} and line $y = n/2$), bending the side of C_{r0} into a polyline, as shown in Fig. 2(b) and (c). Let's take the left side as an example. In order to get n new carriers, drag the point O from two different directions horizontally and symmetrically, and n new turning points O_1, O_2…, O_n can be obtained. The n points are symmetrical with respect to the point O and their line distances satisfy $O_1O_2 = O_2O_3 = \ldots = O_{n-1}O_n$. The n new carriers C_{r1} to C_{rn} corresponding to switches S_{x1} to S_{xn}, respectively. For simplicity, O_1 and O_n are located at the edge and center of a period, respectively, then C_{r1} and C_{rn} turn to be level-shifted two triangular carriers. If n is odd, point O will coincide with point $O_{(n+1)/2}$ and the carrier $C_{r(n+1)/2}$ will coincide with the carrier C_{r0}.

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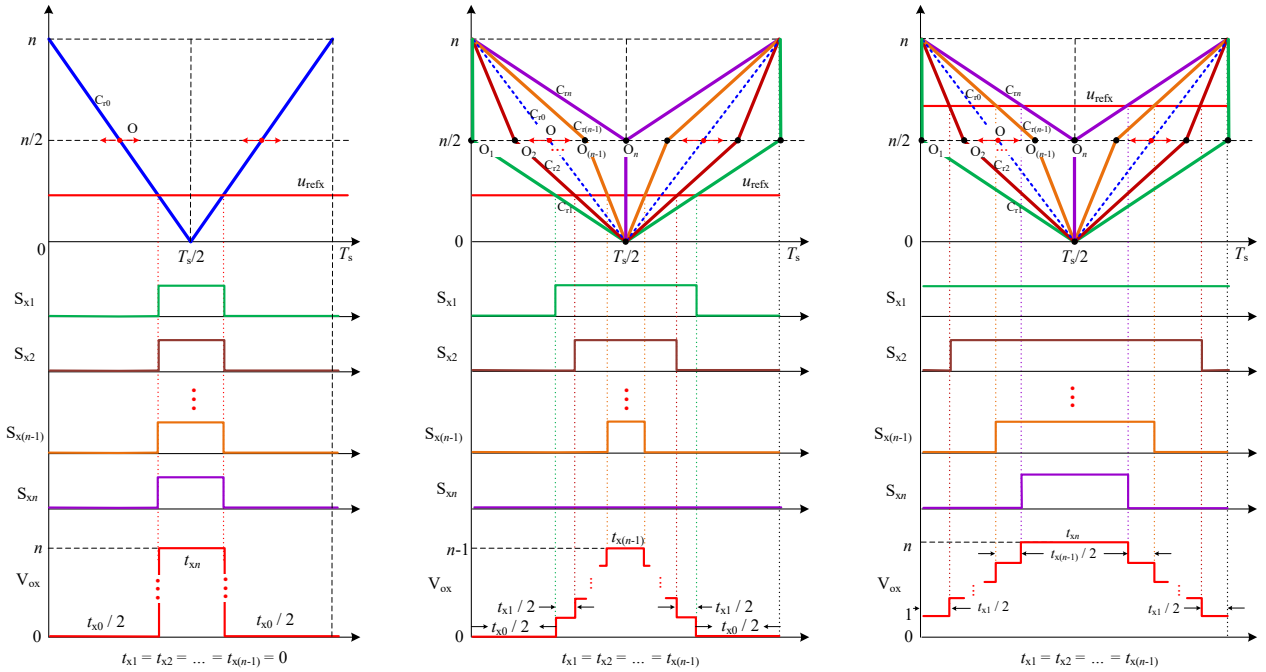

Fig. 2. The derivation of the COPWM: (a) two-level mode, (b) output voltage when $0 \le u_{refx} < n/2$, (c) output voltage when $n/2 \le u_{refx} \le n$.

When a reference voltage u_{refx} that ranges from 0 to n is compared with these new carriers, based on the geometric principle of homothetic triangles, it is easy to deduce that:

$$t_{x1} = t_{x2} = \ldots = t_{x(n-1)}. \tag{2}$$

The time durations of voltage level 0 and n in a carrier period depend on the value range of u_{refx}, as shown in Fig. 2(b) and (c), there are two cases.

Case I: When $0 \le u_{refx} \le n/2$, carrier C_{rn} is always above the reference voltage, as shown in Fig. 2(b). So the time durations of voltage level 0 and n can be obtained as follows:

$$\begin{cases} t_{xn} = 0 \\ t_{x0} = (1 - \dfrac{2u_{refx}}{n}) T_s \end{cases}. \tag{3}$$

Then the time durations of other voltage levels can be deduced:

$$\begin{aligned} & t_{x1} = t_{x2} = \ldots = t_{x(n-1)} \\ & = (1 - t_{x0} - t_{xn}) / (n-1) = \frac{2u_{refx}}{n(n-1)} T_s \end{aligned} \tag{4}$$

Case II: When $n/2 \le u_{refx} \le n$, carrier C_{r1} is always below the reference voltage, as shown in Fig. 2(c). So the time durations of voltage level 0 and n can be obtained as follows:

$$\begin{cases} t_{x0} = 0 \\ t_{xn} = (\dfrac{2u_{refx}}{n} - 1) T_s \end{cases}. \tag{5}$$

Then the time durations of other voltage levels can be deduced:

$$\begin{aligned} & t_{x1} = t_{x2} = \ldots = t_{x(n-1)} \\ & = (1 - t_{x0} - t_{xn}) / (n-1) = \frac{2(n - u_{refx})}{n(n-1)} T_s \end{aligned} \tag{6}$$

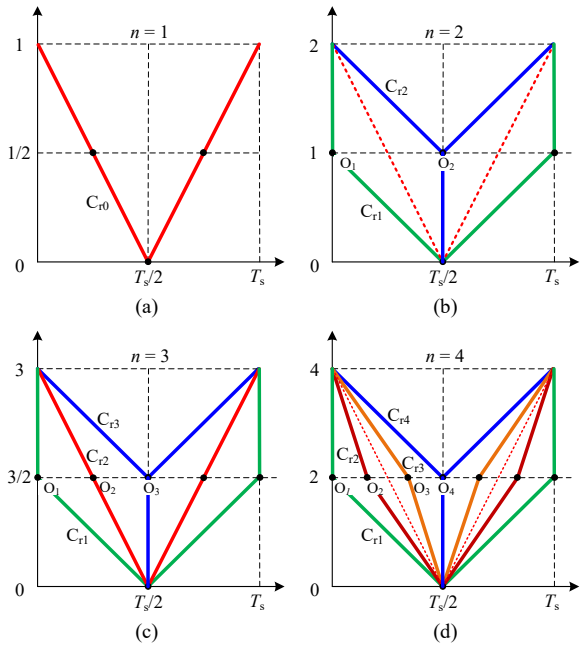

Fig. 3. The diagram of the proposed generalized COPWM for different voltage levels: (a) two-level case, (b) three-level case, (c) four-level case and (d) five-level case.

The proposed COPWM is universal for all the voltage levels. When n=1, it is a single triangular carrier for two-level converters, as shown in Fig. 3(a). When n=2, it is identical to the three-level PDPWM, as shown in Fig. 3(b). When n=3, it

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turns to be the four-level COPWM proposed in [30], as shown in Fig. 3(c). And finally, the five-level COPWM is shown in Fig. 3(d).

(b) The mathematical proof of the natural voltage balance ability

A modulation method is feasible only if it satisfies the voltage-second balance principle. That is to say, the average value of the output voltage in a carrier period must be equal to the reference voltage. In the light of (3) to (6), the average output voltage u_{ox} in a carrier period can be derived as follows.

Case I: When $0 \le u_{refx} \le n/2$, the average output voltage in a carrier period can be calculated as follows.

$$u_{ox} = \frac{1}{T_s}\sum_{j=0}^{n} j \cdot t_{xj} = \frac{n(n-1)}{2} \cdot \frac{2u_{refx}}{n(n-1)} = u_{refx} \tag{7}$$

Case II: When $n/2 \le u_{refx} \le n$, the average output voltage in a carrier period can be calculated as follows.

$$\begin{aligned} u_{ox} &= \frac{1}{T_s}\sum_{j=0}^{n} j \cdot t_{xj} = \frac{n(n-1)}{2} \cdot \frac{2(n-u_{refx})}{n(n-1)} + n \cdot (\frac{2u_{refx}}{n} - 1) \\ &= u_{refx} \end{aligned} \tag{8}$$

From (7) and (8) it can be seen, the average output voltage in a carrier period is equal to the reference voltage in both the two cases, which means the proposed generalized COPWM method satisfies the volt-second balance principle.

Although all the NP currents are equal in a carrier period due to the natural of the COPWM method, the average value must equal zero in a certain period to ensure the NP voltages be naturally balanced in a certain period.

Assume the reference phase voltage and load current are sinusoidal and symmetrical:

$$u_{refx} = n(m\sin\theta + 1)/2, \tag{9}$$

$$i_{ox} = I_m \cdot \sin(\theta - \varphi), \tag{10}$$

where m is the modulation index, θ is the phase angle, I_m is the phase current amplitudes and φ is the power factor angle. In order to improve the dc-link voltage utilization, a 3rd harmonic is commonly used. So in general, the reference voltage can be rewritten as:

$$u_{refx} = n(m\sin\theta + V_z\sin 3\theta + 1)/2, \tag{11}$$

where V_z is the amplitude of the 3rd harmonic component. Then the average NP current in a fundamental period can be calculated as follows:

$$I_{Njx} = \frac{1}{2\pi}\int_0^{2\pi} i_{Njx} d\theta = \frac{1}{2\pi}\int_0^{2\pi} \frac{t_{xj}}{T_s} i_{ox} d\theta, \quad j = 1,2,...,n-1 \tag{12}$$

Fig. 4 shows the curves of the reference voltage and the calculated duty ratio t_{xj}/T_s of NP current when $n = 4$.

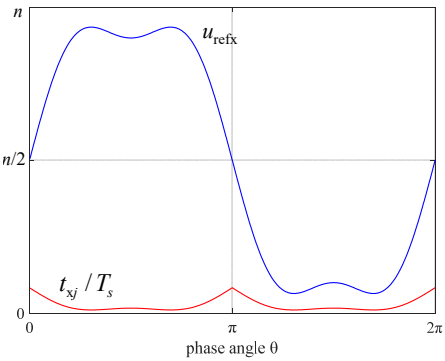

Fig. 4. The reference voltage and the duty ratio of NP current.

Substituting (4) and (6) into (11) and (12), according to the range of θ, the following result can be derived.

$$\begin{aligned} I_{Njx} &= \frac{1}{2\pi}[\int_0^{\pi} \frac{2(n-u_{refx})}{n(n-1)} \cdot i_{ox} d\theta + \int_{\pi}^{2\pi} \frac{2u_{refx}}{n(n-1)} \cdot i_{ox} d\theta] \\ &= \frac{I_m}{2(n-1)\pi}[\int_0^{\pi} (1 - m\sin\theta - V_z\sin 3\theta) \cdot \sin(\theta - \varphi) d\theta \\ &\qquad + \int_{\pi}^{2\pi} (1 + m\sin\theta + V_z\sin 3\theta) \cdot \sin(\theta - \varphi) d\theta] \\ &= 0 \end{aligned} \tag{13}$$

From (13) it can be concluded that the average value of each NP current I_{Njx} in a fundamental period is zero, regardless of the modulation index and power factor, which means that with the proposed generalized COPWM, all the NP voltages can be naturally balanced in a fundamental period under ideal and steady-state conditions.

The idea of this modulation method is similar to the VV PWM method in [24] and [25]. The generated phase voltage and line voltage are also similar. Both of them are defined to maintain the average NP currents equal zero over a specific period of time. The difference is that the period of time considered by the two solutions varies from a switching cycle up to a full line cycle. The main benefit of the VV PWM method in [24] is that the average NP currents equal zero over a single switching cycle, which allows a maximum reduction of the capacitance value or voltage ripples [25].

In the proposed COPWM method, although the average NP currents equal zero over a line cycle for the single-phase circuit, it will be shortened for a three-phase or multi-phase system. Moreover, compared with VV PWM, the switching transitions and losses are also reduced. As shown in Fig. 2, the switches S_{x1} and S_{xn} only act in a half line cycle, so the equivalent switching frequency of S_{x1} and S_{xn} is halved.

(c) The total harmonic distortion comparison

Compared with traditional PDPWM method, although the COPWM has the natural voltage balance ability for NPC multilevel converters, it is achieved at the expense of an increase in the total harmonic distortion (THD) of the output voltages. The harmonic performance of COPWM is worse than PDPWM with the same voltage levels and carrier frequency. However, the THD of COPWM is still lower than that in a two-level converter with sinusoidal PWM (SPWM). The THDs of line voltages under different modulation methods is compared in Table I (The neutral-point voltages are assumed balanced and

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constant). The standard 2L-SPWM, 3-level PDPWM and 5-level PDPWM methods for two-level inverter, three-level NPC inverter and five-level NPC inverter are considered, respectively. Since the output current depends on the line voltage, the THDs of line voltages for different modulation indexes are considered.

Table I The THDs of line voltages under different modulation methods

Modulation methods	THDs		
	m = 0.25	m = 0.5	m = 1.0
2L-SPWM	202.6%	139.5%	52.7%
3L-PDPWM	124.8%	68.1%	27.3%
5L-PDPWM	52.8%	35.1%	14.0%
5L-COPWM	**52.9%**	**41.3%**	**32.2%**

From the comparison it can be seen, for the high modulation index, the THD of 5L-COPWM is higher than 5L-PDPWM. However, it is close to 3L-PDPWM and much lower than 2L-SPWM. For the medium and low modulation indexes, the THD of 5L-COPWM is lower than 3L-PDPWM and 2L-SPWM. Especially when the modulation index is very low, such as 0.25, the THD of 5L-COPWM is nearly the same as 5L-PDPWM. In this regard, the proposed COPWM method is feasible and much better than the solution of two-level or three-level converters with switches connected in series.

III. The Equivalent Multi-reference Modulation Method

Since each carrier is not a triangular but a polyline with different slopes, it is very complex to generate these carriers in a single DSP chip. An equivalent method can be used to generate the same switching signals. The idea is to use n new references to compare with only one triangular carrier to get n switching signals.

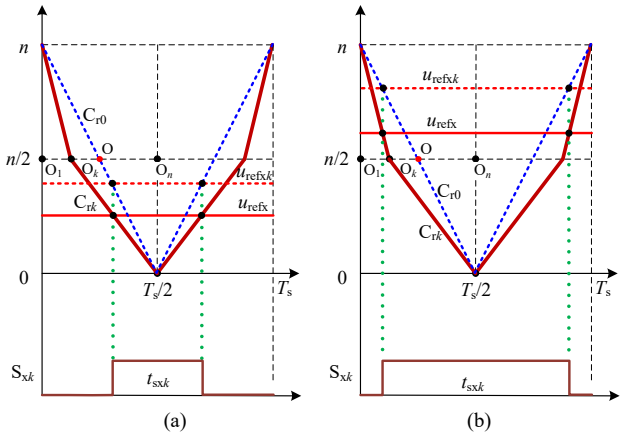

Fig. 5. The diagram of generating the switching signal. (a) $0 \le u_{refx} < n/2$. (b) $n/2 \le u_{refx} \le n$.

Fig. 5 shows the diagram of comparing the reference voltage u_{refx} with carrier C_{rk} to generate the switching signal for S_{xk}, which can be equivalent to comparing a new reference voltage u_{refxk} with the triangular carrier C_{r0} to generate the same switching signal. Based on the geometric principle of homothetic triangles, the new reference voltage can be derived in terms of the range of u_{refx}.

Case I: When $0 \le u_{refx} \le n/2$, as shown in Fig. 5(a), the following equation holds.

$$\frac{OO_n}{O_kO_n} = \frac{u_{refx}}{u_{refxk}} \tag{14}$$

So u_{refxk} can be derived as:

$$u_{refxk} = \frac{2(n-k)}{n-1}u_{refx}, k = 1,2,...,n \tag{15}$$

Case II: When $n/2 \le u_{refx} \le n$, as shown in Fig. 5(b), the following equation holds.

$$\frac{O_1O_k}{O_1O} = \frac{n-u_{refxk}}{n-u_{refx}} \tag{16}$$

So, in this case u_{refxk} can be derived as:

$$u_{refxk} = n - \frac{2(k-1)}{n-1}(n-u_{refx}), k = 1,2,...,n \tag{17}$$

Based on (15) and (17), a set of new reference voltages for all the switches can be obtained. Although it is derived from the generalized COPWM method, it can also be regarded as a new generalized multi-reference modulation method, as shown in Fig. 6. With this method, it is very easy to get n new reference values in a DSP chip. Comparing them with a triangular carrier, n switching signals can be generated easily.

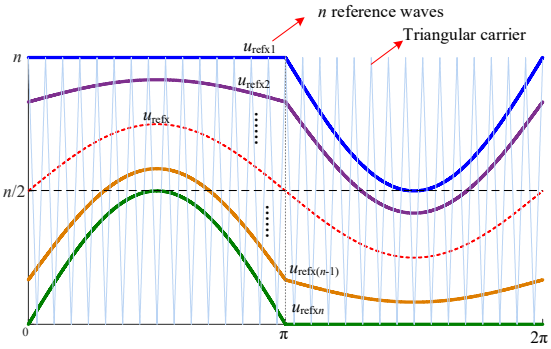

Fig. 6. The generalized multi-reference modulation method.

Since the generalized multi-reference modulation method is equivalent to the COPWM method, it also has the natural voltage balance ability. According to Fig. 6, the time durations of voltage level k (k = 1, 2, …, n-1) in this modulation method can be obtained as follows:

$$t_{xk} = t_{sxk} - t_{sx(k+1)} = \frac{u_{refxk}}{n}T_s - \frac{u_{refx(k+1)}}{n}T_s \tag{18}$$

where t_{sxk} is the duration time of the switching signal for S_{xk}. Substituting (15) and (17) into (18), then the following results can be obtained:

$$t_{xk} = \begin{cases} \dfrac{2u_{refx}}{n(n-1)}T_s, & 0 \le u_{refx} \le n/2 \\ \dfrac{2(n-u_{refx})}{n(n-1)}T_s, & n/2 \le u_{refx} \le n \end{cases} \tag{19}$$

Eq. (19) has no relation with variable k and is identical with (4) and (6), which further proves the equivalence of these two modulation methods.

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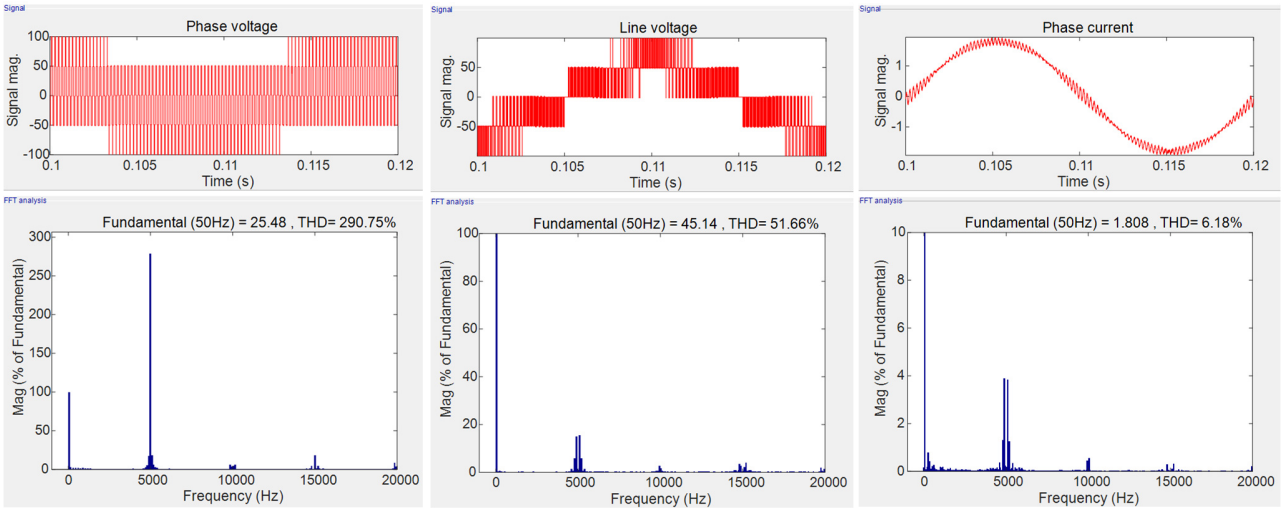
IV. Simulation Results

In order to demonstrate the validity of the proposed modulation method, the simulation and experimental results on a diode-clamped five-level inverter are presented in this paper. The circuit parameters are summarized in Table II.

Fig. 7 shows the simulation waveforms and harmonic spectrums of the phase voltage, line voltage and phase current applying the proposed COPWM method with the modulation index m = 0.25. The line voltage has only five levels due to the low modulation index. It can be observed that most of the harmonic components are concentrated on the carrier-frequency and multiple carrier-frequency. Especially in the phase voltage, there is a large amount of carrier-frequency component. However, it is greatly eliminated in the line voltage and current. Hence, the THDs of the line voltage and phase current are lowered down significantly. Fig. 8 shows the waveforms and harmonic spectrums for m = 0.75. With the increase of the modulation index, the number of the voltage levels of the line voltage is also increased to nine.

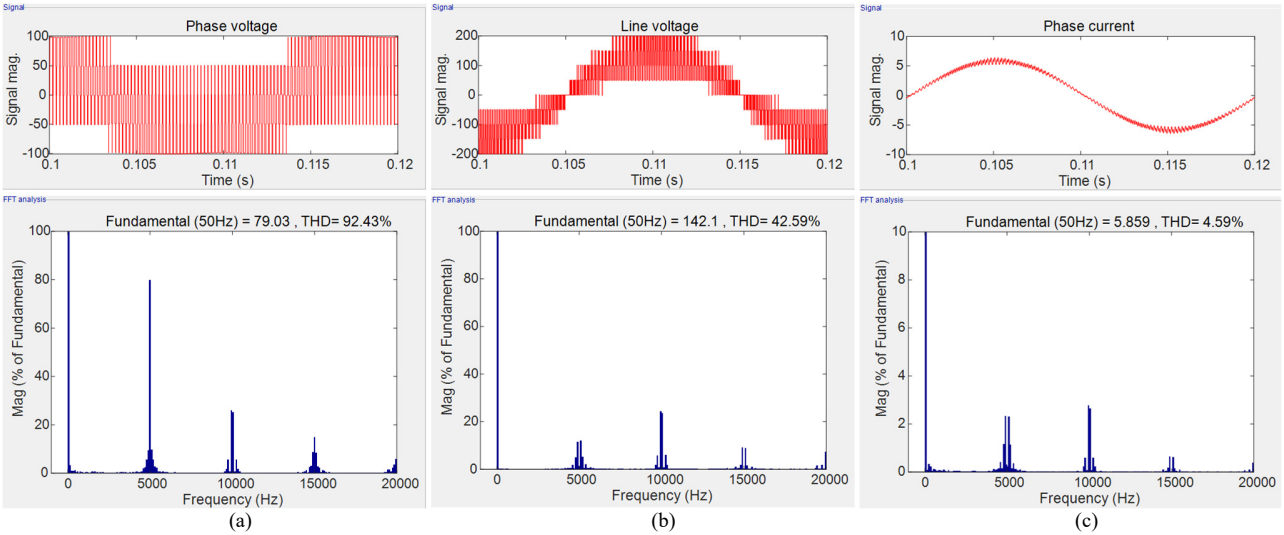
Table II Circuit parameters used for the simulation and experiment

Parameters	Value
DC-link voltage	U_{dc} = 200 V
Nominal capacitor voltage	E= 50 V
DC-link capacitors	$C_{d1} = C_{d2} = C_{d3} = C_{d4}$ = 1410 μF
Carrier frequency	f_c = 5 kHz
R-L load	R = 14 Ω, L = 2 mH,
Power factor	PF = 0.999



(a) (b) (c)

Fig. 7. The simulation harmonic spectrums of (a) the phase voltage, (b) the line voltage and (c) the phase current with m = 0.25.



(a) (b) (c)

Fig. 8. The simulation harmonic spectrums of (a) the phase voltage, (b) the line voltage and (c) the phase current with m = 0.75.

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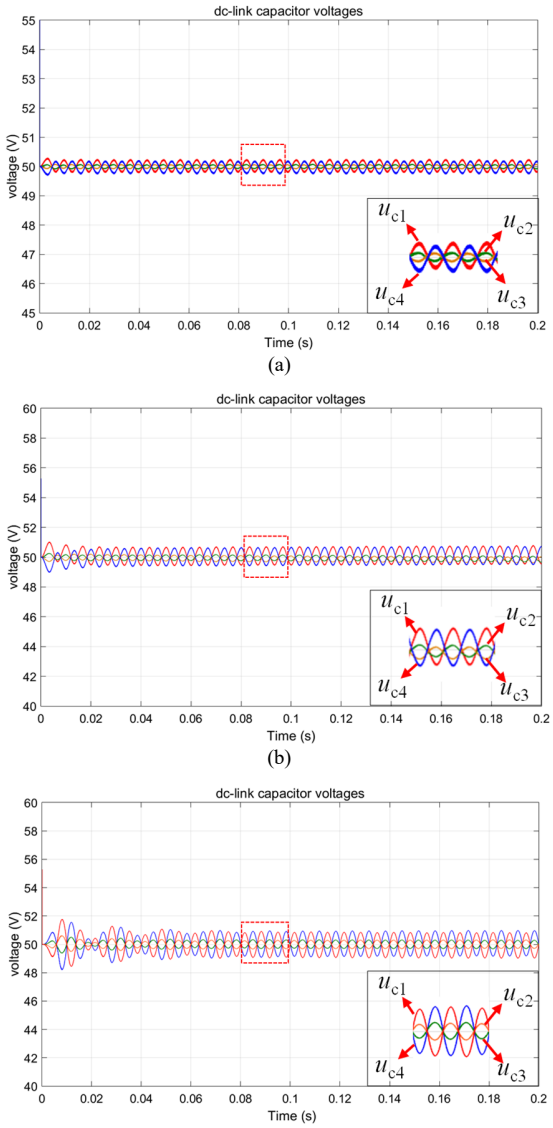
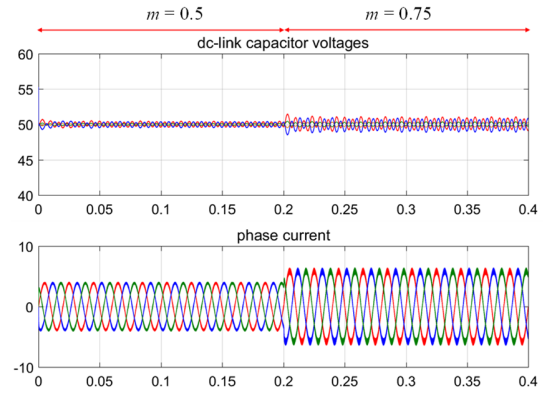


Fig. 9. The four dc-link capacitor voltages under different load conditions: (a) m = 0.25, PF = 0.999, (b) m = 0.75, PF = 0.999, (c) m = 0.75, PF = 0.



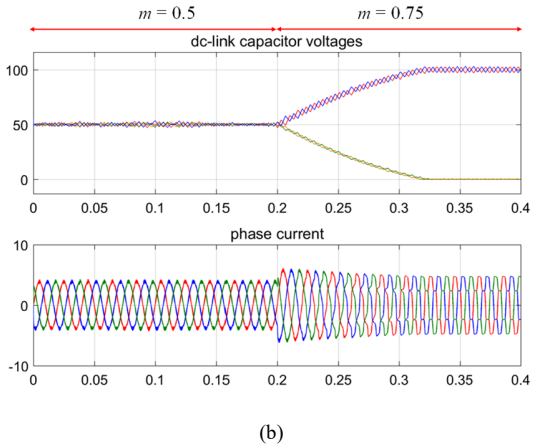


Fig. 10. Dynamic simulation results when the modulation index is stepped up from 0.5 to 0.75. (a) Result of COPWM method; (b) result of PDPWM method.

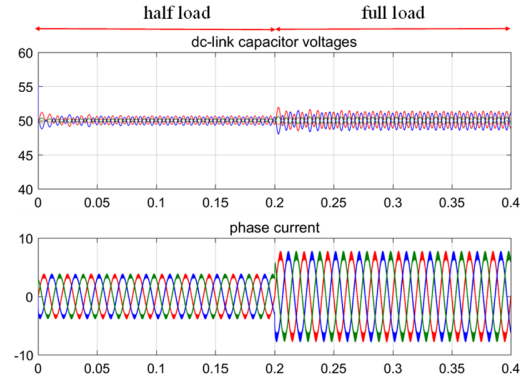


Fig. 11. Dynamic simulation result when the load is doubled.

Fig. 9 shows the four dc-link capacitor voltages under different load conditions, where Fig. 9(a) is the result of m = 0.25, power factor PF = 0.999 (R = 14 Ω, L = 2 mH), Fig. 9(b) is the result of m = 0.75, PF = 0.999, and Fig. 9(c) is the result of m = 0.75, PF = 0 (R = 0 Ω, L = 60 mH). As shown, with the proposed COPWM, all the four dc-link capacitor voltages are well balanced under both low and high modulation indexes and both low and high power factors.

In order to compare the voltage balance performance of the proposed COPWM method and traditional PDPWM method, the dynamic results under COPWM and PDPWM when the modulation index is stepped up from 0.5 to 0.75 are shown in Fig. 10 (a) and (b), respectively. It can be observed clearly that the four dc-link capacitor voltages are balanced very well under COPWM, while divergent under PDPWM. Fig. 11 also shows the dynamic result under COPWM with m = 1.0 when the load is suddenly doubled from half load to full load. The four dc-link capacitor voltages remain balanced.

Although all the NP currents are equal in a carrier period, it can be observed that the voltage ripples of different capacitors are different. The voltage ripples of the upper and lower dc-link capacitors are larger than the two middle capacitors, which is due to the difference of the capacitor currents.

For a single phase of five-level NPC converter, the currents flow out of each dc-link capacitor in a carrier period can be written as follows:

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$$\begin{cases} i_{cd1x} = \frac{3}{4}i_{N1x} + \frac{1}{2}i_{N2x} + \frac{1}{4}i_{N3x} \\ i_{cd2x} = -\frac{1}{4}i_{N1x} + \frac{1}{2}i_{N2x} + \frac{1}{4}i_{N3x} \\ i_{cd3x} = -\frac{1}{4}i_{N1x} - \frac{1}{2}i_{N2x} + \frac{1}{4}i_{N3x} \\ i_{cd4x} = -\frac{1}{4}i_{N1x} - \frac{1}{2}i_{N2x} - \frac{3}{4}i_{N3x} \end{cases} \tag{20}$$

where i_{cd1x}, i_{cd2x}, i_{cd3x} and i_{cd4x} are the discharging currents of four dc-link capacitors C_{d1}, C_{d2}, C_{d3} and C_{d4}.

Because all the NP currents are equal in a carrier period, supposing i_{N1x}= i_{N2x}= i_{N3x}= i_{Nx}, then (20) can be rewritten as follows:

$$\begin{cases} i_{cd1x} = \frac{3}{2}i_{Nx} \\ i_{cd2x} = \frac{1}{2}i_{Nx} \\ i_{cd3x} = -\frac{1}{2}i_{Nx} \\ i_{cd4x} = -\frac{3}{2}i_{Nx} \end{cases} \tag{21}$$

That is to say, the currents flows out of C_{d1} and C_{d4} in a carrier period are three times of that out of C_{d2} and C_{d3}. So the voltage ripples of the upper and lower dc-link capacitors are three times of the two middle dc-link capacitors, which is consistent with the simulation results.

Based on (1), (4), (6) and (21), the amplitude of the capacitor voltage ripple caused by a single phase can be derived by the integration of capacitor current in a positive half cycle:

$$\begin{aligned} \Delta U_{cd1} &= 3\Delta U_{cd2} = -3\Delta U_{cd3} = -\Delta U_{cd4} = \frac{1}{C_d}\int_{T/2} i_{cd1x}dt \\ &= \frac{3}{2\omega C_d}\left[\int_{\varphi}^{\pi}\frac{2(n-u_{refx})}{n(n-1)}\cdot i_{ox}d\theta + \int_{\pi}^{\pi+\varphi}\frac{2u_{refx}}{n(n-1)}\cdot i_{ox}d\theta\right] \\ &= \frac{I_m}{4\omega C_d}\left[\int_{\varphi}^{\pi} 2(1-m\sin\theta - V_z\sin 3\theta)\cdot\sin(\theta-\varphi)d\theta \right. \\ &\qquad \left. + \int_{\pi}^{\pi+\varphi} 2(1+m\sin\theta + V_z\sin 3\theta)\cdot\sin(\theta-\varphi)d\theta\right] \\ &= \frac{I_m}{4\omega C_d}\left[4 - m\cos\varphi(\pi-2\varphi) - m\sin\varphi + \frac{V_z}{4}(3\sin 3\varphi - \sin\varphi)\right] \end{aligned} \tag{22}$$

Eq. (22) shows that the amplitude of the capacitor voltage ripple is related to the modulation index m, power factor angle φ and the 3rd harmonic zero-sequence voltage V_z, inversely proportional to the fundamental frequency ω, which is the same as the traditional three-level NPC converters [33] – [35]. However, for a three-phase system, all the phase currents influence the capacitor currents at the same time. So the frequency of the capacitor currents is triple fundamental-frequency and the voltage ripples can be reduced [33] – [35].

The low-frequency NP voltage oscillations of three-level NPC converters have been studied in many papers [33] – [40]. Since all the NP currents of multilevel NPC converters are equal under the proposed COPWM, the NP voltage oscillation characteristic with COPWM is very similar with the three-level NPC converters. Although all the dc-link capacitor voltages can be naturally balanced in a fundamental period with COPWM, a closed-loop voltage balancing control is needed in practical applications.

Classic zero-sequence voltage injection method can not only be used to balance the NP voltage of three-level NPC converters, but also can suppress the oscillations [40]. It can also be used to enhance the NP voltage balance ability and suppress the low-frequency oscillations under COPWM. A closed-loop voltage balance control method based on COPWM for a four-level ANPC converter is proposed in [41], which achieves the NP voltage balance by zero-sequence voltage injection and slightly adjusting the duty ratios of switching signals. For the NPC converters with more voltage levels, more NP voltages need to be considered, but the idea is similar.

V. Experimental Results

The validity of proposed COPWM method is also demonstrated by experimental results obtained from a low power five-level diode-clamped inverter, as shown in Fig. 12. A DSP chip is used to calculate the three-phase reference voltages and the four carriers are generated in a FPGA. The specifications and circuit parameters are identical with the simulation, and summarized in Table II.

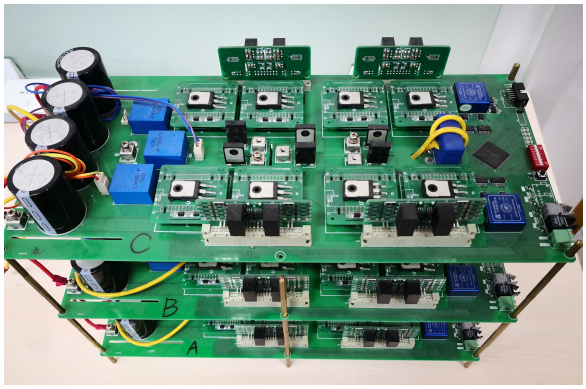

Fig. 12. The experimental prototype of the five-level diode-clamped inverter

Fig. 13 and 14 present the steady-state waveforms with unity power factor (R = 14 Ω, L = 2 mH, PF = 0.999). The modulation indexes are m = 0.25 and m = 0.75, respectively. The waveforms of the phase and line voltages accord with the simulation results very well. Fig. 15 shows the result for m = 0.75 with pure inductance load (R = 0 Ω, L = 60 mH, PF = 0). The four capacitor voltages are stable and balanced under all the conditions, although there are some minor static errors. The reason of the minor voltage drift is that only open-loop control is used and there are lots of non-idealities that can result in capacitor voltage unbalance. Therefore, a closed-loop control need to be further studied in practical applications to improve the voltage balancing performance.

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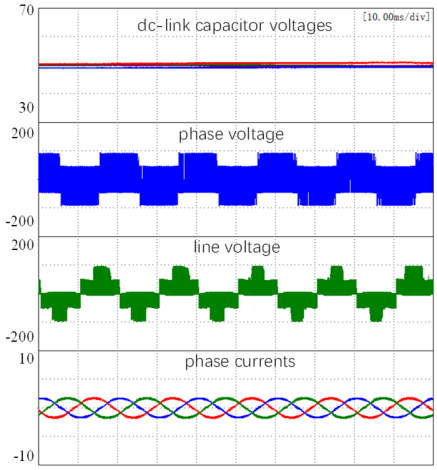


Fig. 13. Experimental results for m = 0.25, PF = 0.999.

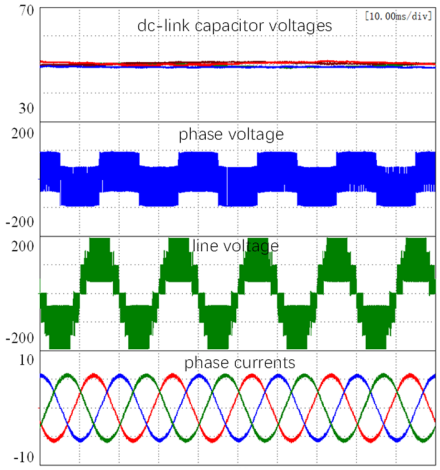


Fig. 14. Experimental results for m = 0.75, PF = 0.999.

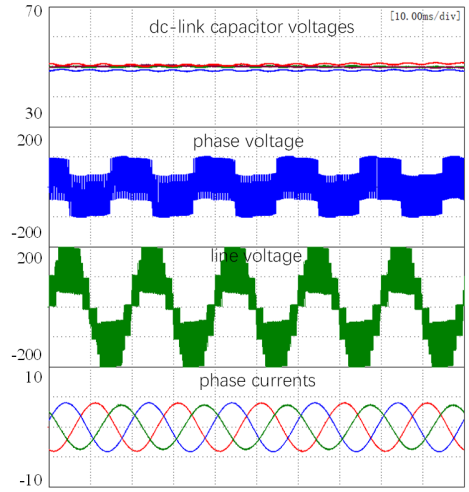


Fig. 15. Experimental results for m = 0.75, PF = 0.

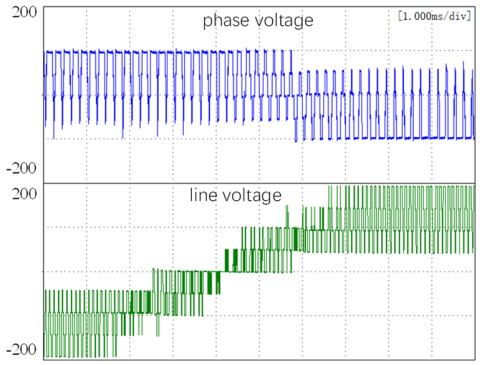
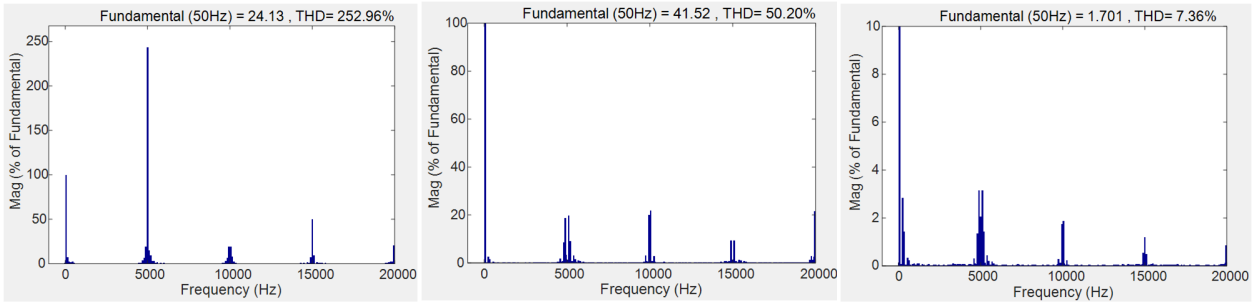
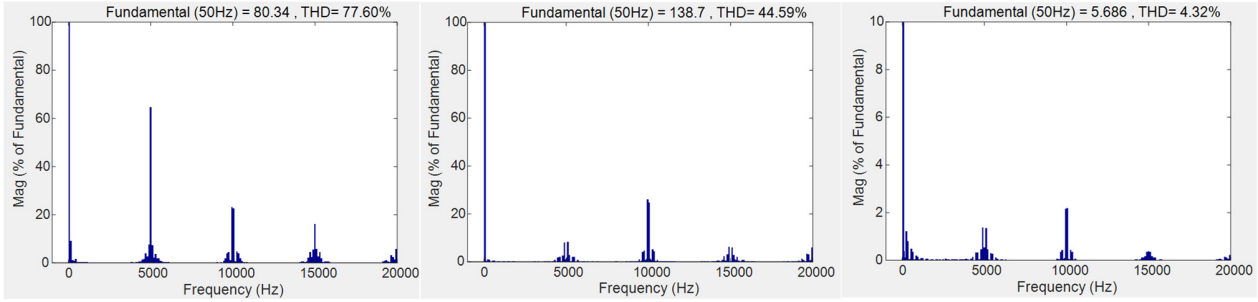


Fig. 16 The detailed waveforms of the phase voltage and line voltage.



(a) (b) (c)

Fig. 17. The experimental harmonic spectrums of (a) the phase voltage, (b) the line voltage and (c) the phase current with m = 0.25.



(a) (b) (c)

Fig. 18. The experimental harmonic spectrums of (a) the phase voltage, (b) the line voltage and (c) the phase current with m = 0.75.

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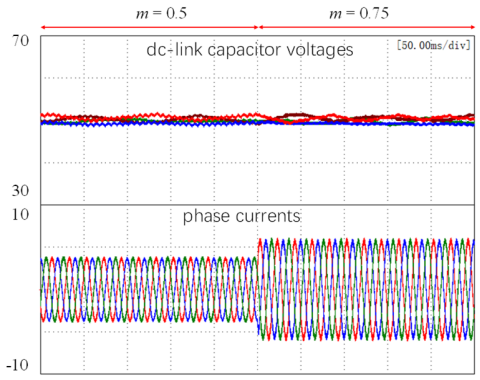
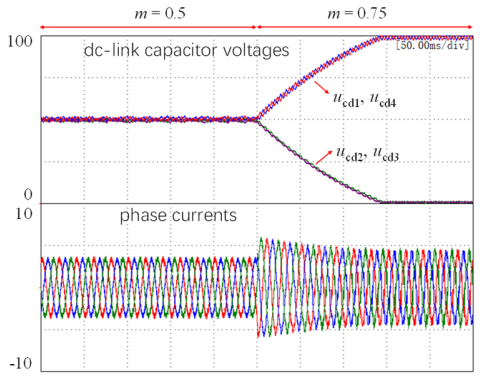
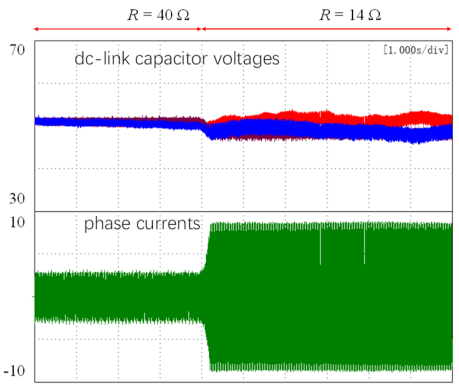


(a)



(b)

Fig. 19. Dynamic experimental results when the modulation index is stepped up from 0.5 to 0.75. (a) Result of COPWM method; (b) result of PDPWM method.



(c)

Fig. 20. Dynamic experimental result of sudden load change.

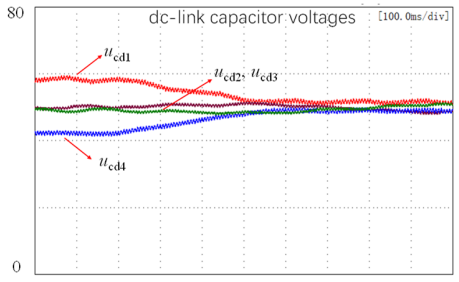


Fig. 21. Experimental result with unequal initial voltages.

Fig. 16 shows the detailed waveforms of phase voltage and line voltage for m = 0.75, which agrees with the theoretical waveforms given in Fig. 7 very well. The line voltage involves two-level and three-level variations during a carrier period, which is similar to that in [27] and [28].

Fig. 17 and Fig. 18 presents the harmonic spectrums of the phase voltage, line voltage and phase current for m = 0.25 and m = 0.75 with the unity power factor load. Compared with the simulation results in Fig. 7 and Fig. 8, the harmonic spectrums and THDs are in good agreement with the simulation. Although there are lots of harmonics around the carrier-frequency and multiple carrier-frequency, there is no obvious low-order harmonics, and the high-frequency components are very easy to be filtered.

Fig. 19 to Fig. 21 show the dynamic performance of COPWM. The comparison between the proposed COPWM and the traditional PDPWM is shown in Fig. 19. When the modulation index is stepped up from 0.5 to 0.75, the four dc-link capacitor voltages remain balanced very well under COPWM, but loss balance quickly under PDPWM. This result also agrees with the analysis in [14], which gives the limits of voltage balance of the traditional SVM-based balancing method for a five-level NPC inverter. Generally, the neutral-point voltages cannot be balanced for unity power factor load under traditional NTV or PDPWM method when the modulation index exceeds 0.55, whereas COPWM method breaks this limit easily.

Fig. 20 shows the voltage balancing performance of COPWM with m = 1.0 when the load is suddenly increased from light load to full load. Although there exists a small voltage drift due to the dynamic load change, the four dc-link capacitor voltages remain roughly balanced during the whole process.

Fig. 21 shows the experimental result with unequal initial voltages. The initial voltages of the upper and lower dc-link capacitors are 20% higher and 20% lower than the nominal voltages by different paralleled resistors. It can be observed that the two voltages converge gradually at last.

The simulation and experimental results on the five-level NPC inverter show that the proposed COPWM method has a good natural capacitor voltage balance ability. Compared with traditional NTV and PDPWM methods, the COPWM can achieve the neutral-point voltage balancing over the full range of power factors and modulation indexes. Compared with the methods in [27] and [28], the voltage balancing performances under different modulation indexes are similar. However, the COPWM method is much easier to implement, which is the most significant advantage of this method. However, due to the non-ideal factors such as dynamic load change, dead-time, current distortion, etc., a small voltage drift may occurs. Therefore, a closed-loop control based on this COPWM also needs to be studied to enhance the voltage balance performance.

VI. Conclusion

In order to solve the neutral-point voltage balance problem of multilevel NPC converters, a novel generalized carrier-

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overlapped PWM (COPWM) is proposed in this paper. Started with the two-level modulation, a set of bended carriers are deduced geometrically to acquire the same time duration for different voltage levels, which ensures the same NP currents under the COPWM method. By analyzing the average output voltage in a carrier period, it is proven that the proposed generalized COPWM method satisfies the volt-second balance principle. Furthermore, by calculating the average value of the NP currents, it is found that the average value of each NP current equals zero in a fundamental period, indicating that the dc-link capacitor voltages can be naturally balanced in a fundamental period. In order to simplify its implementation, an equivalent generalized multi-reference modulation method is also derived, which employs only one triangular carrier and has the same characteristics with COPWM.

The main drawback of this modulation method is increased THD and switching losses. It is an unavoidable expense to achieve the voltage balancing. However, compared with other modulation methods with the same carrier frequency, the THD of 5L-COPWM is close to 3L-PDPWM and much lower than 2L-SPWM. In this regard, the proposed COPWM method is much better than the solutions of two-level or three-level converters with switches connected in series. Moreover, as the fast development of high-speed wide bandgap semiconductors such as SiC devices, the two drawbacks will be greatly relieved. Simulation and experimental results on a five-level NPC inverter demonstrate the validity of this modulation method.

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Kui Wang (M'11-SM'19) was born in Hubei, China, in 1984. He received the B.S. and Ph.D. degrees in Electrical Engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2006 and 2011, respectively. He is currently an Assistant Researcher with the Department of Electrical Engineering, Tsinghua University. His research interests include topology and control of multilevel converters, renewable energy generation and wide band-gap semiconductor applications.

Zedong Zheng (M'09-SM'19) was born in Shandong, China, in 1980. He received the B.S. and Ph.D. degrees in Electrical Engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2003 and 2008, respectively. He is currently an Associate Professor with the Department of Electrical Engineering, Tsinghua University. His research interests include power electronics transformers and high-performance motor control systems.

Lie Xu (M'11) was born in Beijing, China, in 1980. He received the B.S. degree in electrical and electronic engineering from the Beijing University of Aeronautics and Astronautics, Beijing, China, in 2003, and the M.S. and Ph.D. degrees in Electrical and Electronic Engineering from The University of Nottingham, Nottingham, U.K., in 2004 and 2008, respectively. From 2008 to 2010, he was a Research Fellow with the Department of Electrical and Electronic Engineering, The University of Nottingham. He is currently an Associate Professor with the Department of Electrical Engineering, Tsinghua University, Beijing, China. His research interests include multilevel converters, direct ac–ac power conversion, and multilevel matrix converter.

Yongdong Li (M'08-SM'19) was born in Hebei, China, in 1962. He received the B.S. degree in electrical engineering from Harbin Institute of Technology, China, in 1982 and the M.S. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Institut National Polytechnique de Toulouse, Toulouse, France, in 1984 and 1987, respectively. Since 1996, he has been a Professor with the Department of Electrical Engineering, Tsinghua University, Beijing, China. His research interests include power electronics, machine control, and transportation electrification.

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